ABSTRACT OF THE DISCLOSURE

A semiconductor memory device has an array of memory cells for memorizing data, an address circuit responsive to an address signal for addressing a memory cell in the array, and a write circuit responsive to a write signal for writing the data into the addressed memory cell. A control circuit is provided for delaying an input timing of the write signal to the write circuit by a given delay amount so as to adjust a timing of writing the data after addressing the memory cell. The control circuit has a register and a variable delay. The register is capable of registering control data for setting the delay amount. The variable delay is provided for delaying the write signal by the set delay amount and outputting the delayed write signal to the write circuit.